A MICROWAVE MINIATURIZED LINEARIZER USING A PARALLEL DIODE

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Abstract

A miniaturized linearizer using a parallel diode has been developed. It is composed of a parallel diode and a resistance for d.c. bias feed. The linearizer utilizes a nonlinear resistive element of the diode. In this paper, the operation principle of the linearizer is described. The parallel diode provides a high temperature stability and readiness of bias voltage adjustment. By applying this linearizer to an S-band power amplifier, an improvement of ACP of 5dB and power added efficiency of 8.5 % has been achieved for the π/4-shift QPSK modulated signal.

Introduction

There are increasing demands for highly efficient and linear microwave power amplifiers as a key component in mobile and satellite communication systems [1,2]. To achieve high efficiency and low distortion simultaneously, we have presented a miniaturized FET linearizer with a source inductor [3] and a series diode linearizer [4], which have small size and simple configurations.

In this paper, we introduce a miniaturized linearizer using a parallel diode. This linearizer provides positive amplitude and negative phase deviations. It is caused by a nonlinearity of the diode and a movement of a bias point.

We apply this linearizer to an S-band power amplifier. The power amplifier with the linearizer includes a variable gain buffer amplifier. The buffer amplifier controls input power of the power amplifier and gives a high isolation between the linearizer and the power amplifier. With this linearizer an improvement of Adjacent Channel leakage Power (ACP) of 5 dB and power added efficiency of 8.5 % has been achieved for the π/4-shift QPSK modulated signal.

Operation principle of a parallel diode linearizer

This linearizer utilizes a nonlinearity of a resistance of the diode in forward bias conditions. A schematic diagram of this linearizer is shown in Fig.1 It is comprised of a parallel Schottky diode with an equivalent resistance R_d and a junction capacitance C_j, two capacitors for d.c. block, and a bias feed resistance R_b. Anode voltage of the diode V_d and d.c. current through the diode I_d are indicated in Fig.1. Figure 2 shows a movement of a bias point. In Fig.2 a point S is a small signal bias point and a point L is a large signal bias point. At the point S, d.c. current through the diode $I_d=I_{ds}$ and anode voltage of the diode $V_d=V_{ds}$ are given by

$$I_{ds} = f(V_{ds}) \qquad \text{at the point S} \qquad (1)$$
$$V_{ds} = V_{cc} - R_b I_{ds}$$

where V_{cc} is power supply voltage and the function f(V) indicates the I-V characteristic of the diode.

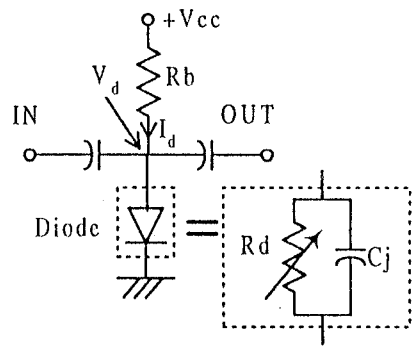

Fig.1 Schematic diagram of a miniaturized linearizer

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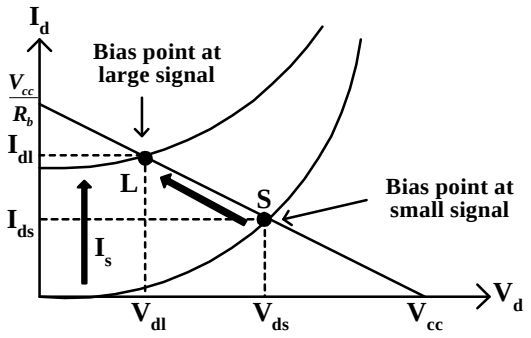

Fig.2 Movement of a bias point

With the increase of input power, a rectified current I_s increases because the current wave is clipped. At the point L, d.c. current through the diode $I_d=I_{dl}$ and anode voltage $V_d=V_{dl}$ are given by

$$I_{dl} = I_s + f(V_{dl}) \quad \text{at the point L} \qquad (2)$$
$$V_{dl} = V_{cc} - R_b I_{dl}$$

Equations (1),(2) indicate that the bias point is changed from the point S to the point L with the increase of input power shown in Fig.2. We can verify in Fig.3 that the measured anode voltage V_d decreases for input power. As a result, R_d increases for input power.

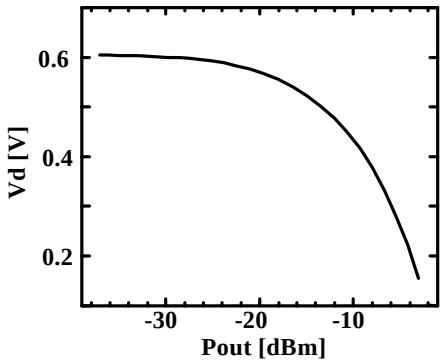

Fig.3 Variation of V_d for output power of the linearizer

From the simplified equivalent circuit of this linearizer in Fig.1, S_{21} of the circuit is given by

$$S_{21} = \frac{2R}{(2R+Z_o)^2 + (C_j R Z_o)^2}\{(2R+Z_o) - j\ C_j R Z_o\} \qquad (3)$$

where

$$R = \frac{R_d \cdot R_b}{R_d + R_b}$$

and Zo is a characteristic impedance. Gain ($|S_{21}|$) and phase ($\angle S_{21}$) are derived from the equation (3) and given by

$$|S_{21}| = \frac{2}{\sqrt{\left(2+\frac{Z_o}{R}\right)^2 + (C_j Z_o)^2}} \qquad (4)$$

$$\angle S_{21} = \tan^{-1}\left(-\frac{C_j Z_o}{2+\frac{Z_o}{R}}\right)$$

From the equation (4), we can find that this linearizer achieves positive amplitude and negative phase deviations with the increase of R. The calculated results of gain and phase with respect to R at 2.7 GHz are shown in Fig.4. In this calculation, C_j is assumed to be constant of 1.5 pF because a variation of C_j can be negligible, as compared with variation of R.

It is clear in this section that this linearizer achieves positive amplitude and negative phase deviations with the increase of input power because of the movement of a bias point and anonlinearity of the diode.

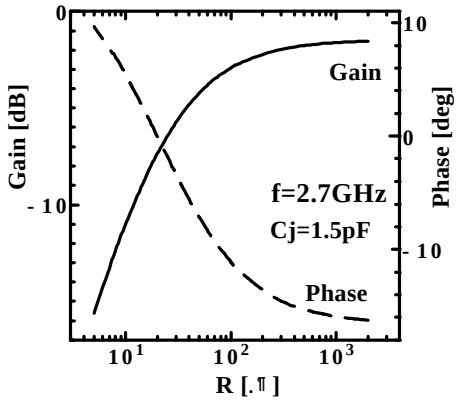

Fig.4 Calculated gain and phase deviations of S_{21}

Characteristics of the power amplifier with the linearizer

Based on this principle, the linearizer has been fabricated to compensate for the distortion of an S-band power amplifier. Figure 5 shows a block diagram of the power amplifier with the linearizer. It is comprised of the miniaturized linearizer using a parallel diode, the variable gain buffer amplifier and the S-band power amplifier. The buffer amplifier is employed instead of an isolator and a level control circuit. The power amplifier has a linear gain of 30.5 dB and a saturated output power of 37.5 dBm at 2.7 GHz.

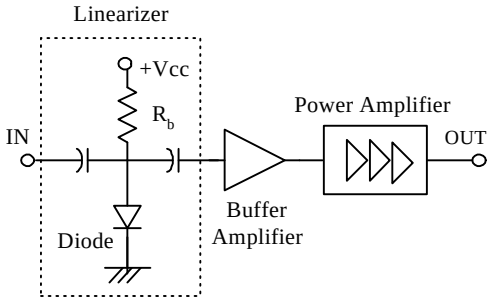

Fig.5 Block diagram of the power amplifier with the linearizer

To demonstrate the capability of this linearizer, the characteristics of the amplifier in following three conditions are measured.

condition-A: without the linearizer (idle current I_{do}=1 A)

condition-B: without the linearizer in low current conditions (I_{do}=0.52 A)

condition-C: with the linearizer in low current conditions (I_{do}=0.52 A)

It is expected in lower current conditions that the power amplifier in condition-C achieves the same distortion as that of the power amplifier in condition-A. Figure 6 shows the measured relative gain and phase of the linearizer with the buffer amplifier. We can verify that this linearizer achieves positive amplitude and negative phase deviations for input power.

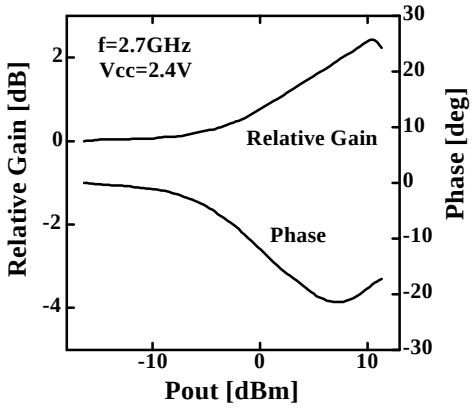

Fig.6 Measured relative gain and phase of the linearizer with the buffer amplifier

Figure 7 shows the measured relative gain and phase deviation of the power amplifier in condition-A, -B, and -C. Figure 8 shows measured ACP of the power amplifier in condition-A,-B, and -C for the 32 kbps π/4 shift QPSK modulated signal at 28.6 kHz offset with a bandwidth of 16 kHz. The amplitude and phase deviations, and ACP of the power amplifier in condition-B become worse than those of power amplifier in condition-A at output power of 34.1 dBm. We can find in Fig.8 that this linearizer compensates for the distortion of the power amplifier in condition-B. ACP has been improved by 5 dB and the power amplifier in condition-C achieves the same ACP as that of the power amplifier in condition-A. Table 1 shows total power added efficiency (η_{add}) and ACP of the amplifier in each condition at output power of 34.1 dBm. In condition-C, the added power efficiency is calculated with including the linearizer. An improvement of η_{add} of 8.5 % has been achieved. The high efficiency and low distortion power amplifier has been obtained with this linearizer.

Table 1 Total power added efficiency and ACP of the power amplifier in each condition

	ACP	η_{add}
condition-A	-36.7dBc	29.3%
condition-B	-31.5dBc	37.9%
condition-C	-36.5dBc	37.8%

* at output power of 34.1dBm,

*η_{add} is calculated with including the linearizer in condition-C

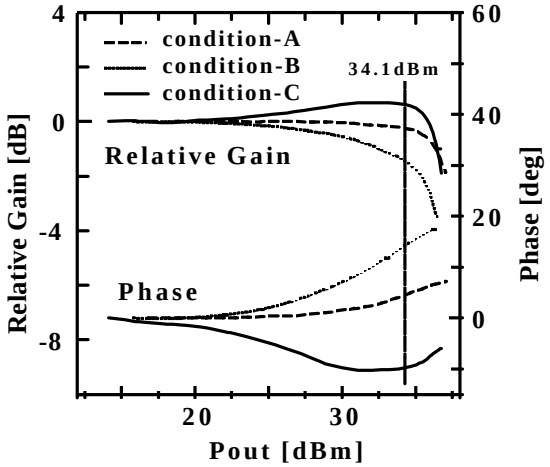

Fig.7 Measured relative gain and phase of the power amplifier

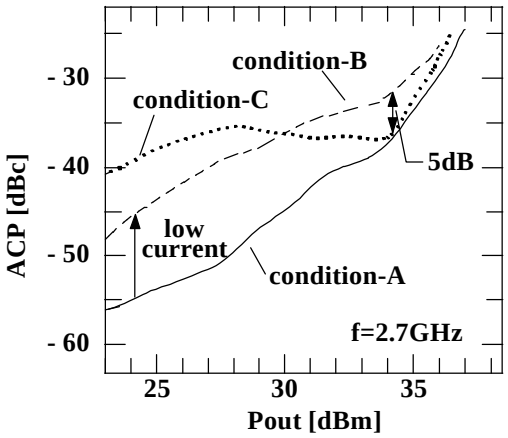

Fig.8 Measured ACP of the power amplifier

Conclusion

A miniaturized linearizer using a parallel diode has been developed. It is composed of a parallel diode and a resistance for d.c. bias feed. This linearizer utilizes the nonlinear resistive element of the diode. With the increase of input power a rectified current increase, and the equivalent resistance of the diode increase. As a result, this linearizer achieves positive amplitude and negative phase deviations. The parallel diode provides the high temperature stability and readiness of bias voltage adjustment. By applying this linearizer to an S-band power amplifier, an improvement of ACP of 5 dB and power added efficiency of 8.5 % has been achieved for the π/4-shift QPSK modulated signal.

References

[1] M.Nakayama, T.Umemoto, Y.Itoh , and T.Takagi, "1.9GHz High-Efficiency Linear MMIC Amplifier", Proceedings of 1994 Asia-Pacific Microwave Conference, pp.347-350.

[2] T.Yokoyama, T.Kunihisa, H.Fujimoto, H.Takehara, K.Ishida, H.Ikeda , and O.Ishikawa, "High-efficiency Low Adjacent Channel Leakage Power GaAs Power MMIC for 1.9GHz Digital Cordless Phones, "IEEE Trans. on Microwave Theory & Tech. , vol.42, No.12, pp.2623-2628, December 1994.

[3] M.Nakayama, K.Mori, K.Yamauchi, Y.Itoh , and T.Takagi, "A Novel Amplitude and Phase Linearizing Technique for Microwave Power Amplifiers", IEEE MTT-S Digest, pp.1451-1454, 1995

[4] K.Yamauchi, K.Mori, M.Nakayama, Y.Itoh, and Y.Mitsui, "A Novel Series Diode Linearizer for Mobile Radio Power Amplifiers", IEEE MTT-S Digest, pp.831-834, 1996